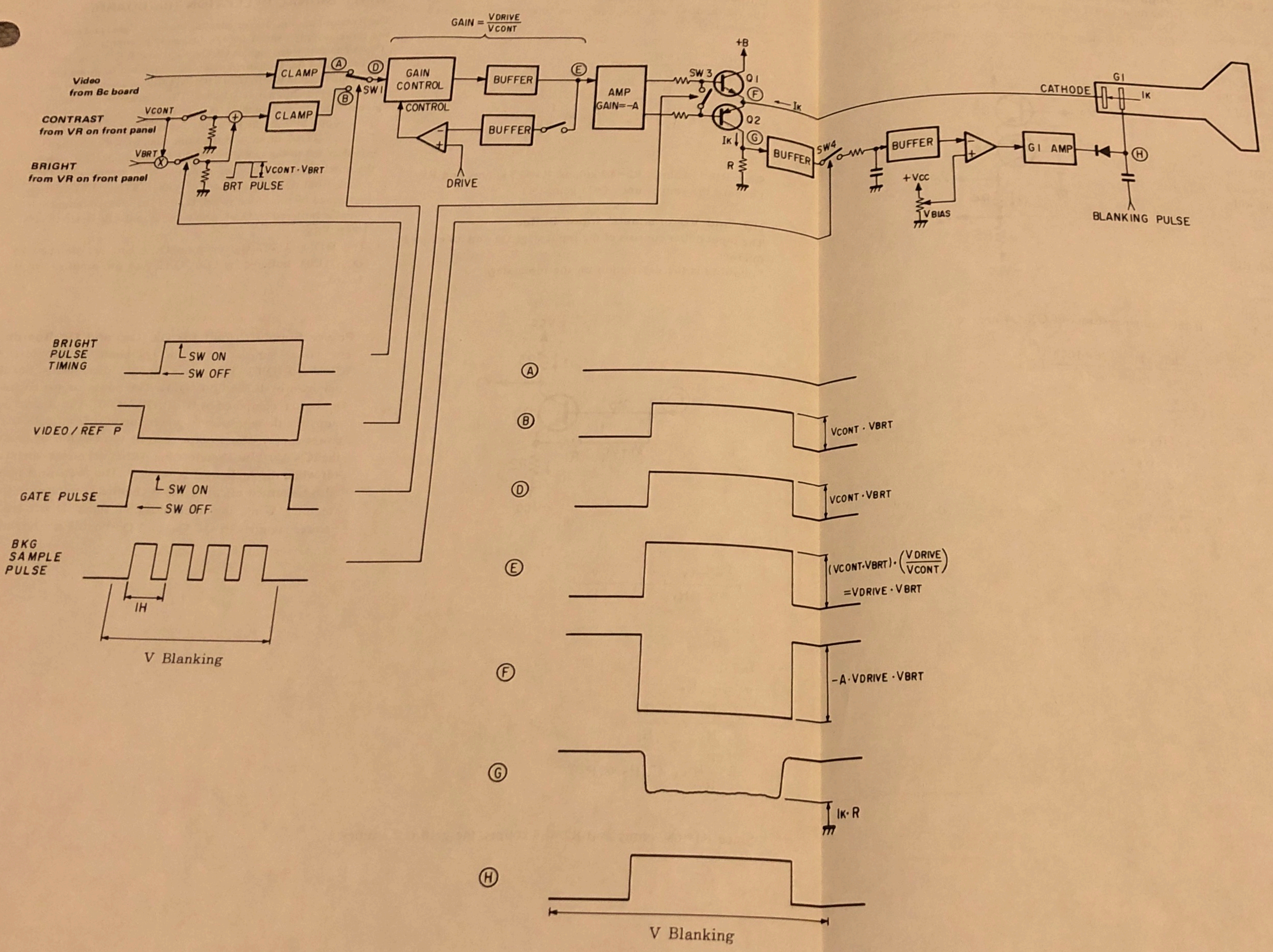


GAIN = VDRIVE / VCONT
Video from Bc board
CLAMP
CONTRAST from VR on front panel
VCONT
BRIGHT from VR on front panel
VBRT
BRT PULSE
VCONT·VBRT
SW1
GAIN CONTROL
CONTROL
BUFFER
DRIVE
AMP GAIN=−A
SW3
+B
Q1
Q2
Ik
R
CATHODE
G1
BUFFER
SW4
+Vcc
VBIAS
G1 AMP
BLANKING PULSE
BRIGHT PULSE TIMING
SW ON
SW OFF
VIDEO / REF P
GATE PULSE
BKG SAMPLE PULSE
1H
V Blanking
VCONT · VBRT
(VCONT·VBRT)·(VDRIVE/VCONT)
=VDRIVE · VBRT
−A·VDRIVE · VBRT
Ik·R
V Blanking

FLOATING TYPE INPUT BUFFER (Q_A, Q_B, Q_C BOARD)

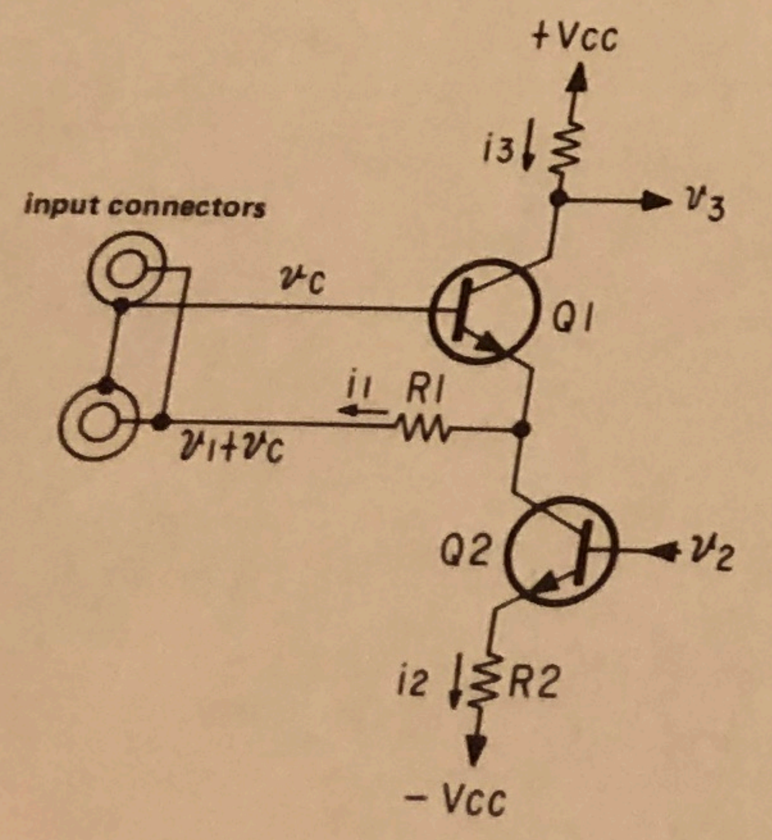
The captioned three circuit boards are connected to the BNC input connectors, having the input buffer function.
These three boards receives power supply from the B_A board. As input signal is selected by the INPUT A, B select switch, etc., the selected circuit board alone receives power supply while the other circuit boards receive no power as power is turned off by the input selector switch.

R, G, B, EXT SYNC channels' Input Buffer

The input buffer circuit comprises the input stage Q1, Q2, the cascode connected high gain amplifier Q3, Q4 and the emitter follower. The negative feedback is applied to form the wide band-width amplifier.

Input Stage

The input signal (v1+vc) is applied to Q1 emitter through R1 while the ground (vc) of the input signal is connected to Q1 base. This circuit configuration can remove the common mode noise of the input signal. The output signal (v2) from the output buffer is fed back to Q2 base. Gain is shown in the equation 1 .



$$i_1=\frac{v_c-(v_1+v_c)}{R_1}=-\frac{v_1}{R_1}$$

The voltage across R1 becomes V1.
(Vc is removed.)

$$i_2=\frac{v_c}{R_2}$$

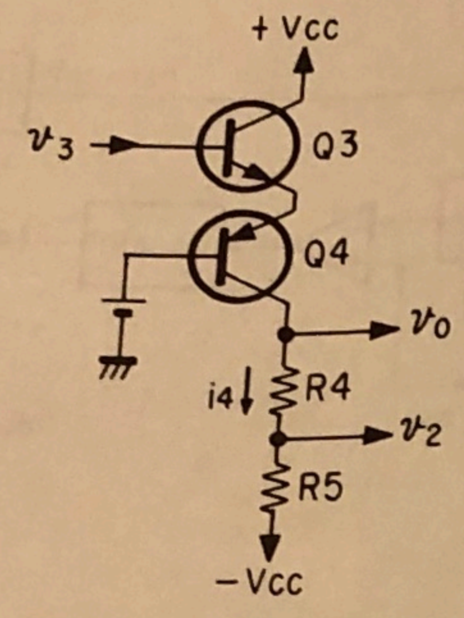
$$i_3=i_1+i_2$$

$$v_3=-i_3R_3$$

$$=\frac{R_3}{R_1}v_1-\frac{R_3}{R_2}v_2 \quad \cdots\cdots\cdots\cdots ①$$

High gain amplifier

The input signal v3 is input to Q3 base. Output is obtained from Q4 collector.
Gain of this stage is shown in equations ②, ③.



If the emitter resistors of Q3, Q4 are "re",

$$re=\frac{kT}{q}\frac{1}{Ic}=\frac{26\times10^{-3}}{Ic}\ (\Omega)$$

$$i_4=\frac{v_3}{2re}$$

$$v_0=i_4(R_4+R_5)$$

$$=\frac{R_4+R_5}{2re}\cdot v_3 \quad \cdots\cdots\cdots\cdots ②$$

$$v_2=\frac{R_5}{2re}v_3 \quad \cdots\cdots\cdots\cdots ③$$

Output Buffer's total gain

The v2 and v3 are removed from the above calculated equations ①, ②, ③.

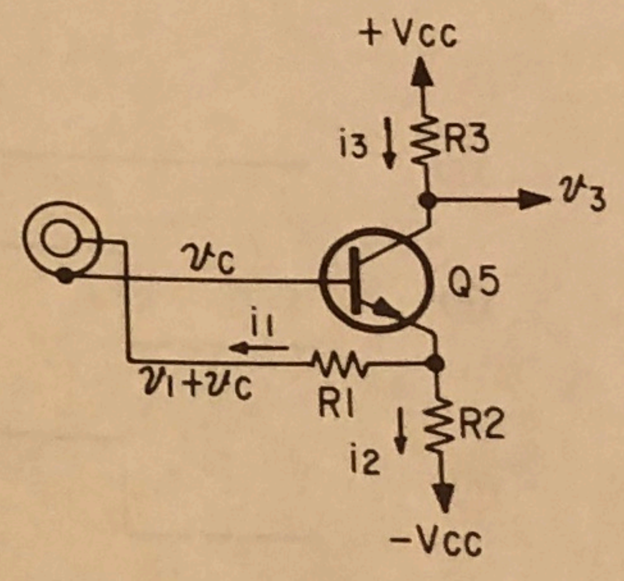
$$v_0=\frac{R_3}{R_1}\frac{R_4+R_5}{2re+\frac{R_3}{R_2}\cdot R_5}v_1$$

$$=\frac{R_2}{R_1}\left(1+\frac{R_4}{R_5}\right)\cdot v_1 \quad (\because 2re\ll\frac{R_3}{R_2}\cdot R_5)$$

Since R1=13 kohms, R2=4.7 kohms, R4=2.2 kohms and R5=1 kohms, the gain is unity (=1) gain.

HD, and VD channels' Input Buffer

The input buffer consists of the input stage Q5 and an emitter follower.
Following is the description on the input stage.



$$i_1=\frac{v_C-(v_1+v_C)}{R_1}=-\frac{v_1}{R_1}$$

$$i_2=\frac{v_C}{R_2}$$

$$i_3=i_1+i_2$$

$$v_3=-i_3R_3$$

$$=\frac{R_3}{R_1}v_1-\frac{R_3}{R_2}v_C$$

$$=\frac{R_3}{R_1}v_1 \quad (\because R_3\ll R_2)$$

Since R1=680 ohms and R2=1.5 kohms, the gain is 2.2 times.

INPUT SIGNAL SELECTION (B_A BOARD)

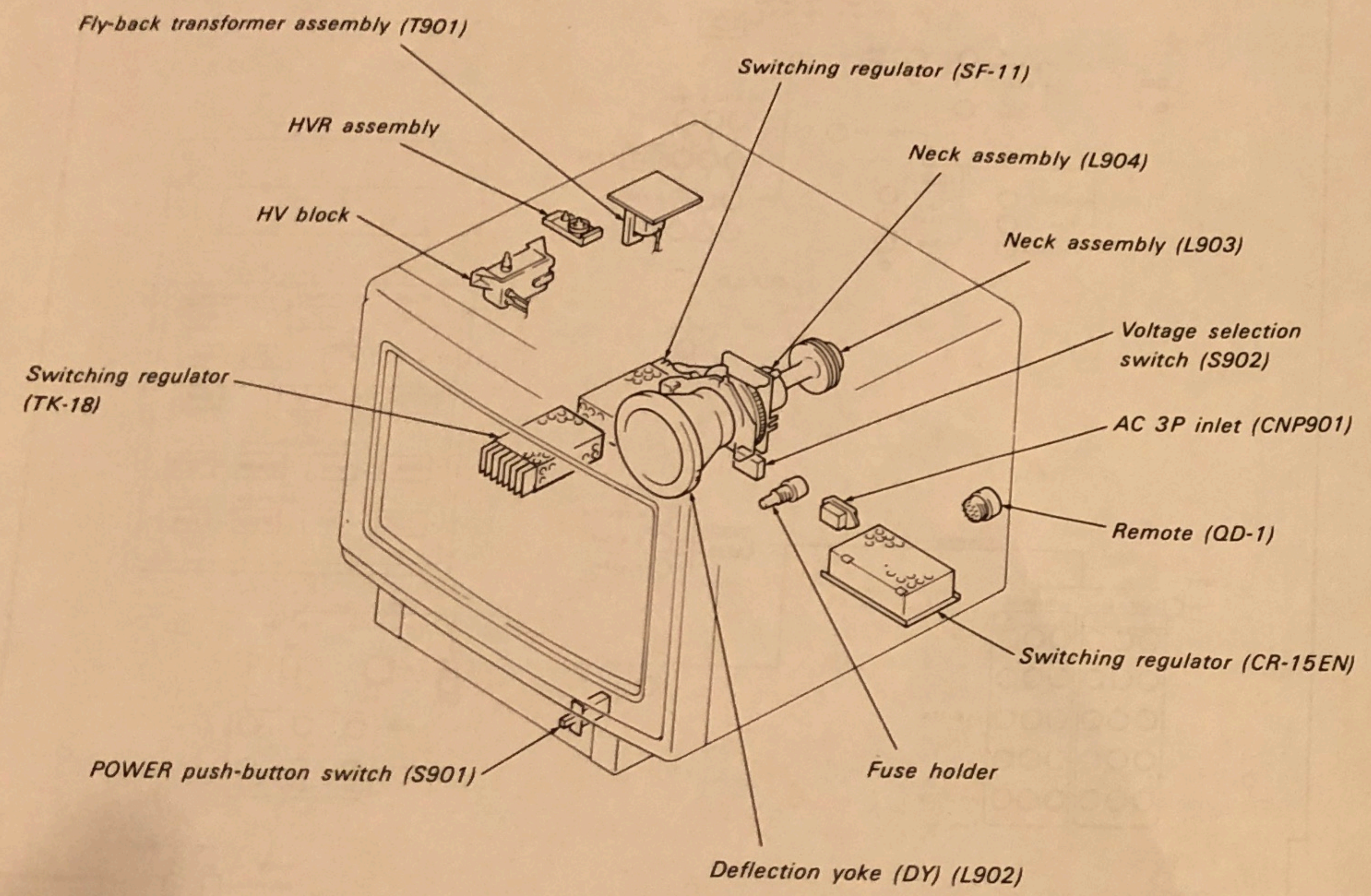
The B_A board has function of selecting the input signal and also the power supply control for Q_A, Q_B, and Q_C boards.
The A-channel video signals (R/C_W, G/Y, and B/C_N) from the Q_A board and the B-channel video signals (ditto) from the Q_B board are input to IC101/IC102/IC103 (LA7016) where either A-channel or B-channel is selected. The selected output video signal from these switching ICs, is buffered by Q101, Q102, Q103, is output from the B_A board and is input to the B_B board.
The EXT SYNC input is at the same time routed from the Q_C board, is fed to the one input of the video switch IC202, while the other input of this video switch IC202 is receiving the G/Y signal from Q102. Selection of either SYNC INT/EXT is performed by this video switch IC202. The selected output sync signal is buffered by Q203, and is input to the B_F board (SYNC PROCESS).
The HD and VD signals from Q_C board are clamped by D201/D203, buffered by Q201/Q202 and are input to the B_F board.

Power Supply Circuit for Q_A, Q_B, and Q_C Boards

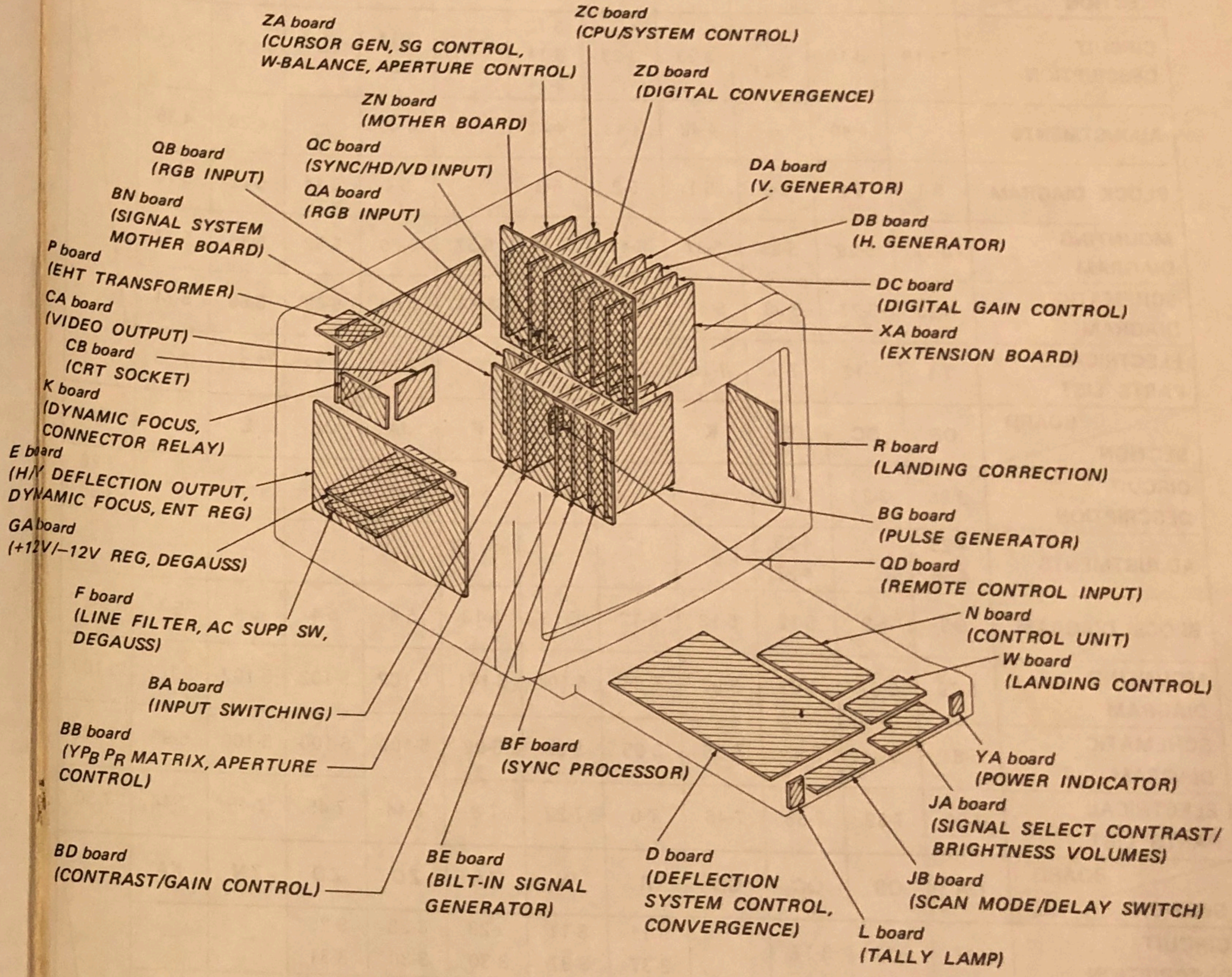
The power supply circuit for Q_A board is composed by IC305/Q301/Q302. The power supply circuit for Q_B board is composed by IC306/Q303/Q304. The power supply circuit for Q_C board is composed by IC307/Q306/Q307. The original power suppy the these respective power supplies, is the ±9V tracking power supply whose output can be turned OFF by grounding the IC's ⑧ pin. Therefore the B-channel power can be turned off while the A-channel is selected. The A-channel power can also be turned off while the B-channel is selected in the same manner. When the internal TEST signal is selected. all the power supplies to Q_A, Q_B, and Q_C boards are turned off.

SECTION 4
ADJUSTMENT

4-1. INTERNAL VIEW DIAGRAM



4-2. BOARD ARRANGEMENT DIAGRAM



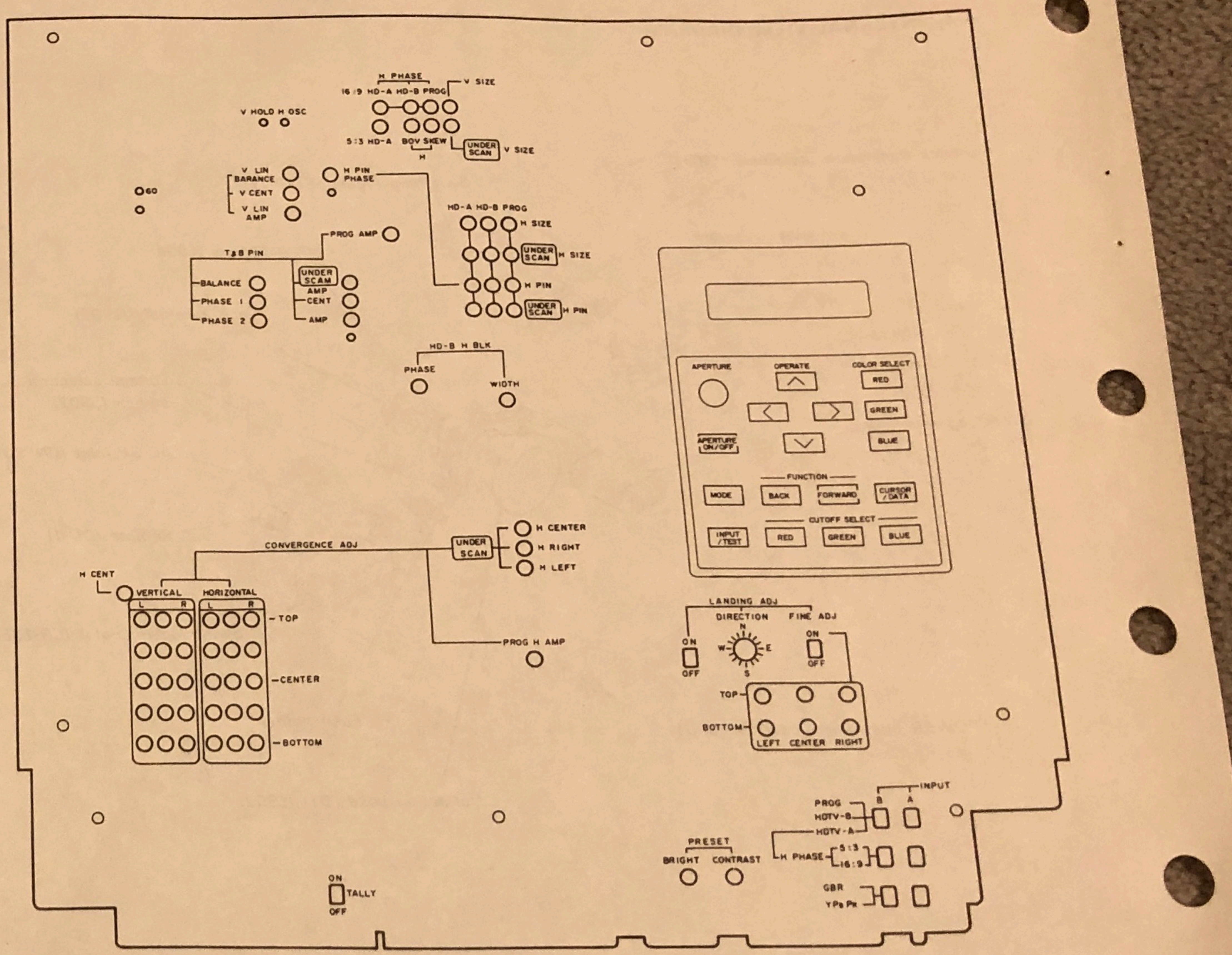
4-3. QUICK REFERANCE

SECTION \ BOARD	BA	BB	BD	BE	BF	BG	BN	CA	CB	D	DA
CIRCUIT DESCRIPTION	3-18	3-19	3-12 3-21	3-23	3-23	3-12 3-14 3-24	–	3-14 3-27	–	3-1	3-32
ADJUSTMENTS	–	4-40	–	4-42	4-43	4-47	–	4-49	–	4-28	4-35
BLOCK DIAGRAM	5-1	5-1	5-3	5-1	5-2	5-3	–	5-4	5-14	5-12	5-10
MOUNTING DIAGRAM	5-21	5-29	5-35	5-37	5-45	5-47	5-57	5-60	5-62	5-66	5-77
SCHEMATIC DIAGRAM	5-23	5-27	5-33	5-39	5-42	5-49	5-54	5-63	5-65	5-69	5-74
ELECTRICAL PARTS LIST	7-1	7-12	7-3	7-15	7-23	7-20	7-1	7-23	7-23	7-37	7-38

SECTION \ BOARD	DB	DC	E	K	P	GA	F	JA	JB	L	Y	N
CIRCUIT DESCRIPTION	3-36	3-38	3-7	–	–	3-10	3-9	–	–	–	–	3-28 3-30
ADJUSTMENTS	4-25 4-36	–	4-25 4-27	–	–	–	–	–	–	–	–	–
BLOCK DIAGRAM	5-9	5-9	5-12	5-13	5-12	5-13	5-13	5-4	5-4	5-4	5-4	5-6
MOUNTING DIAGRAM	5-79	5-87	5-91	5-90	5-90	5-101	5-101	5-102	5-102	5-102	5-102	5-103
SCHEMATIC DIAGRAM	5-81	5-84	5-93	5-95	5-95	5-99	5-99	5-100	5-100	5-100	5-99	5-105
ELECTRICAL PARTS LIST	7-30	7-32	7-33	7-46	7-6	7-22	7-8	7-44	7-45	7-46	7-44	7-50

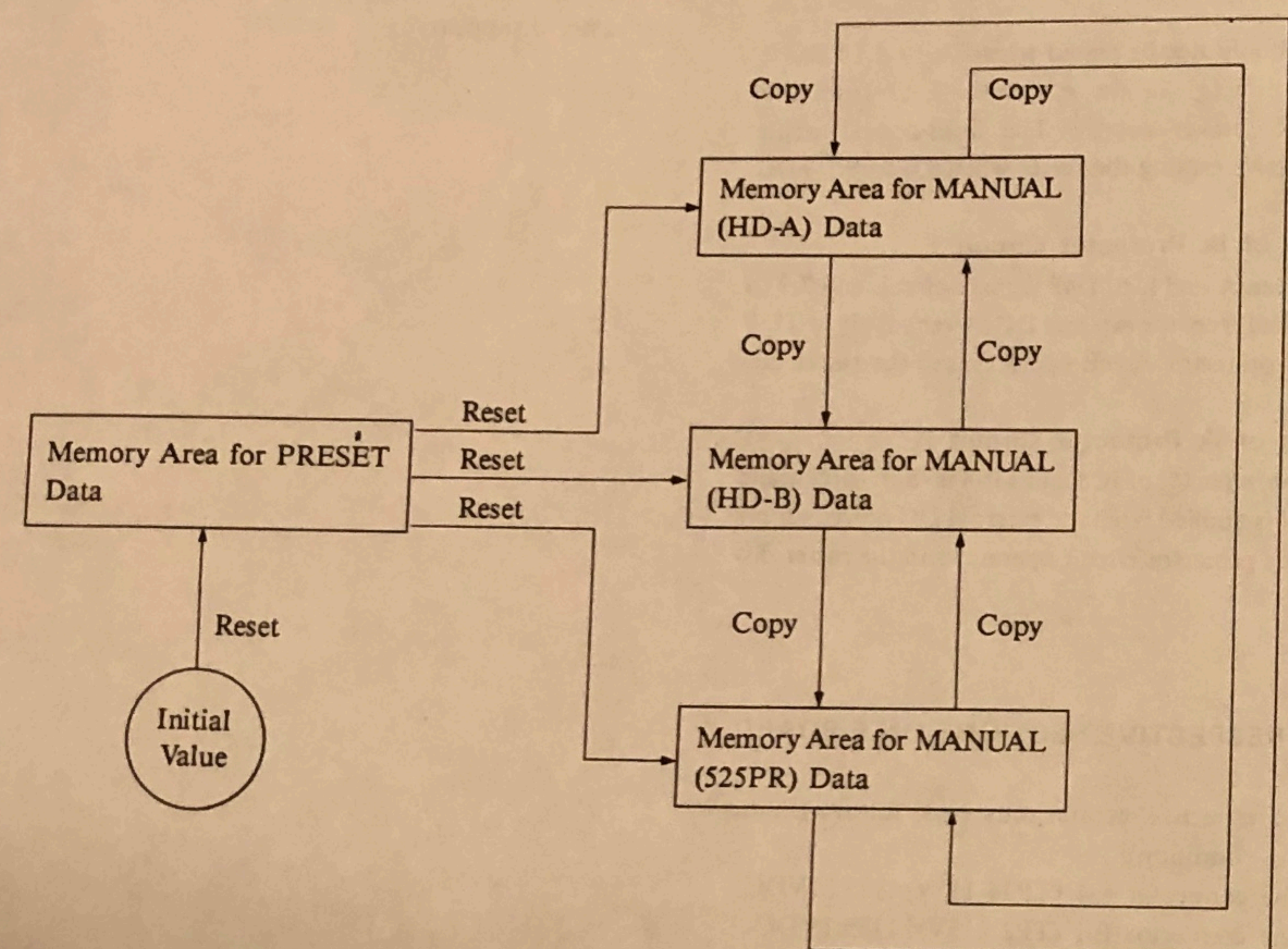
SECTION \ BOARD	QA	QB	QC	QD	R	W	ZA	ZC	ZD	ZN	XA
CIRCUIT DESCRIPTION	3-17	3-17	3-17	–	3-11 3-37	3-11 3-37	3-28 3-30	3-28 3-30	3-28 3-31	–	–
ADJUSTMENTS	4-38	4-38	4-38	–	4-25	4-25	–	–	–	–	–
BLOCK DIAGRAM	5-1	5-1	5-1	5-1	5-14	5-13	5-7	5-6	5-7	–	–
MOUNTING DIAGRAM	5-107	5-107	5-107	5-108	5-112	5-114	5-121	5-123	5-131	5-137	5-139
SCHEMATIC DIAGRAM	5-109	5-109	5-109	5-109	5-115	5-116	5-118	5-125	5-128	5-134	–
ELECTRICAL PARTS LIST	7-10	7-11	7-9	7-10	7-6	7-44	7-46	7-48	7-49	7-46	7-45

4-4. SUB CONTROL PANEL

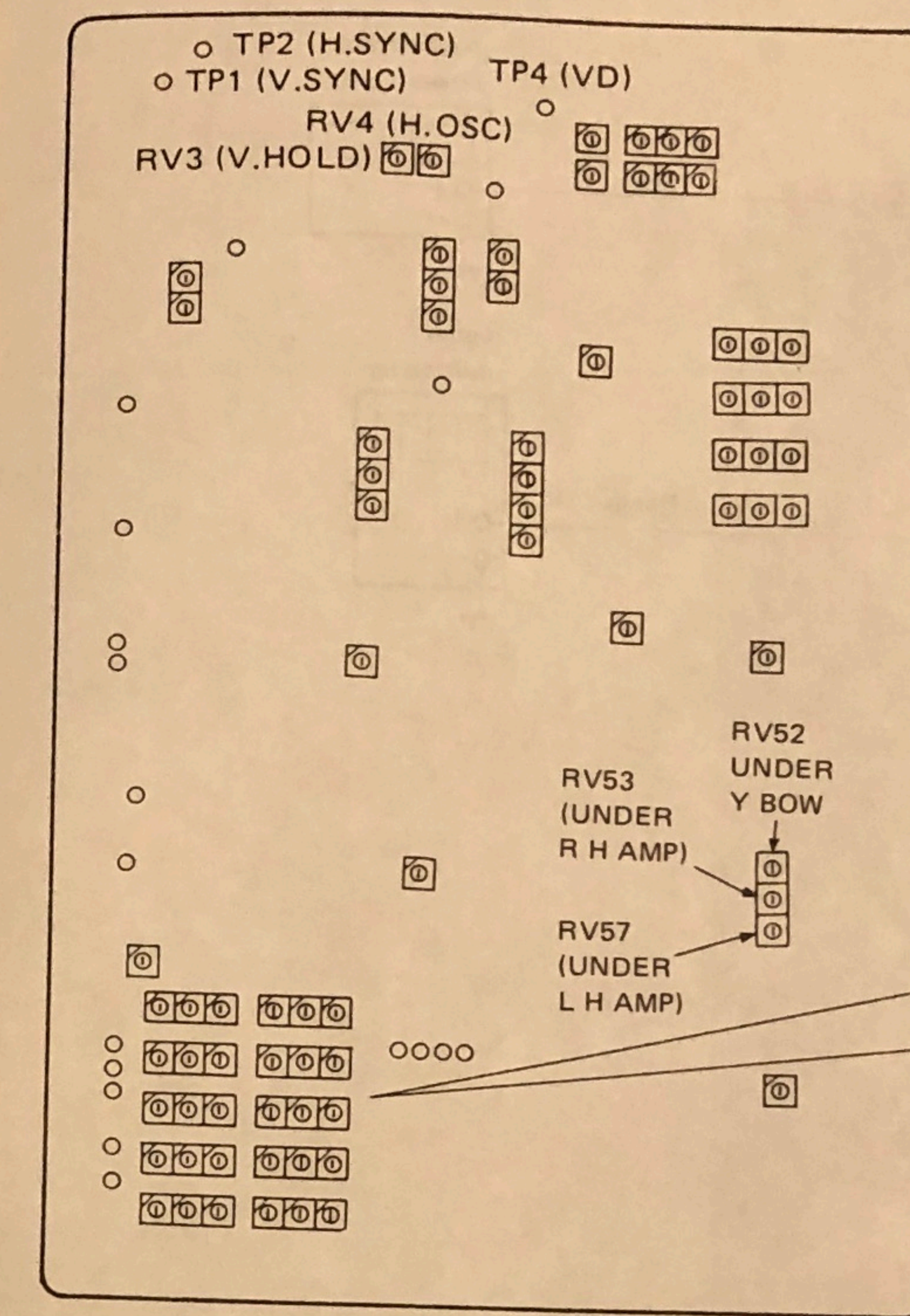


III. Resetting and Copying the Color Temperature Data It is possible to reset and copy the color temperature data in each memory area.

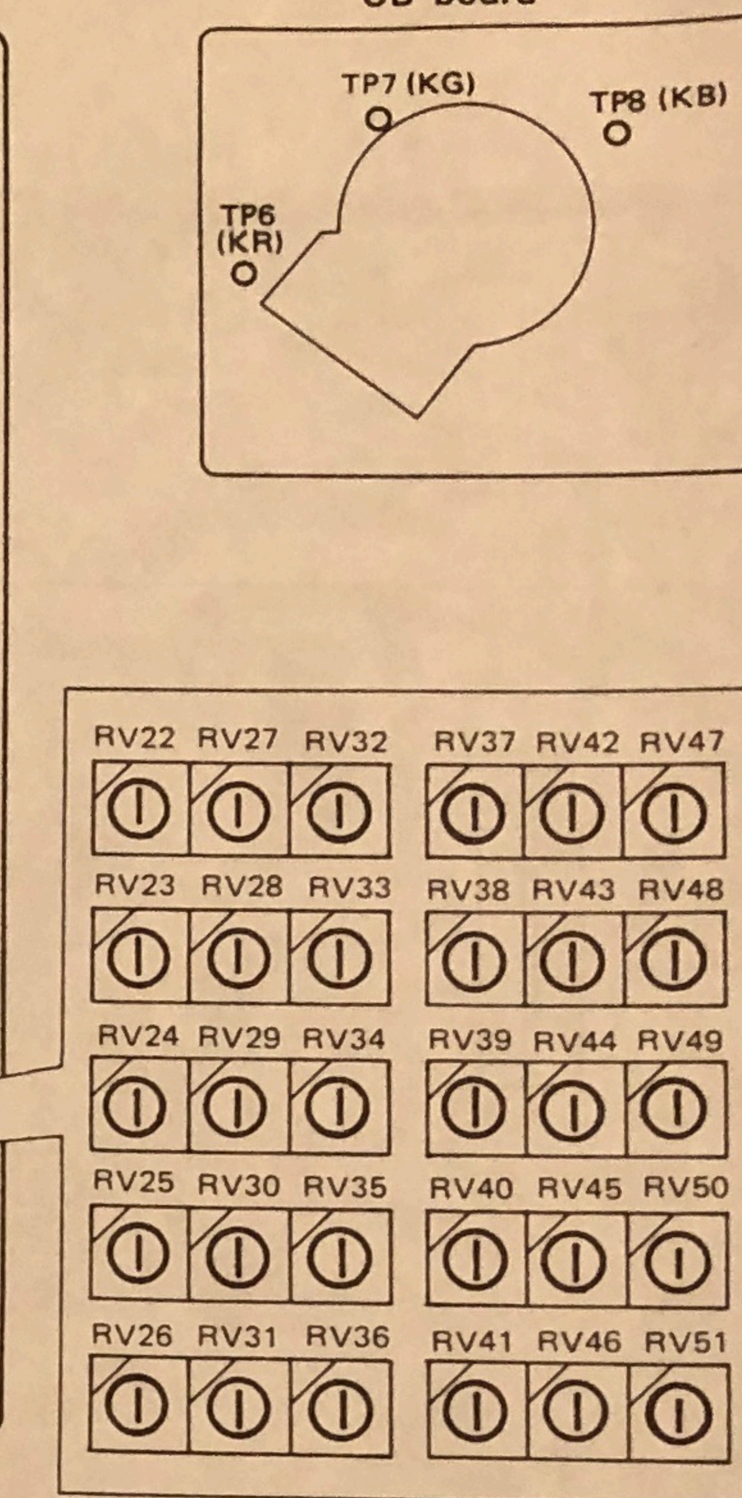
All the data (BIAS 1, BIAS 2 and GAIN data for R, G and B respectively) in the memory area are simultaneously reset and copied. The resetting and copying methods are referred to in "1-5-4. Resetting of Adjustment Data" and "Copying of Color Temperature" in "1-5-2. Color Temperature Adjustment".



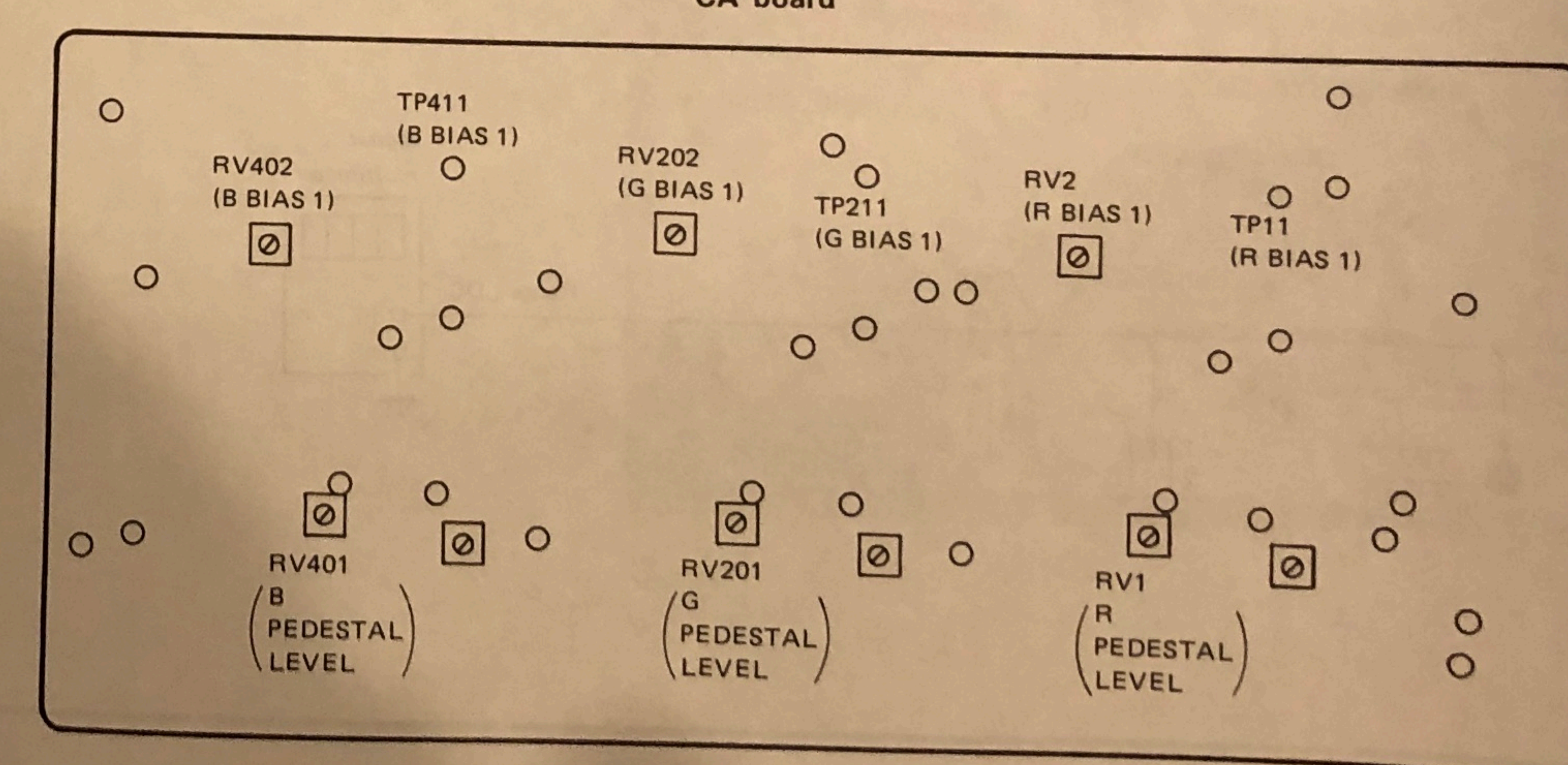
D board



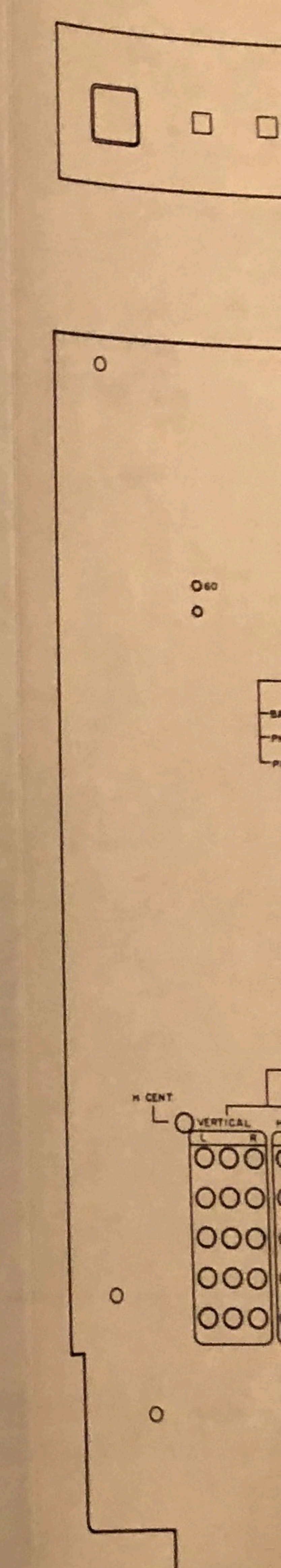
CB board

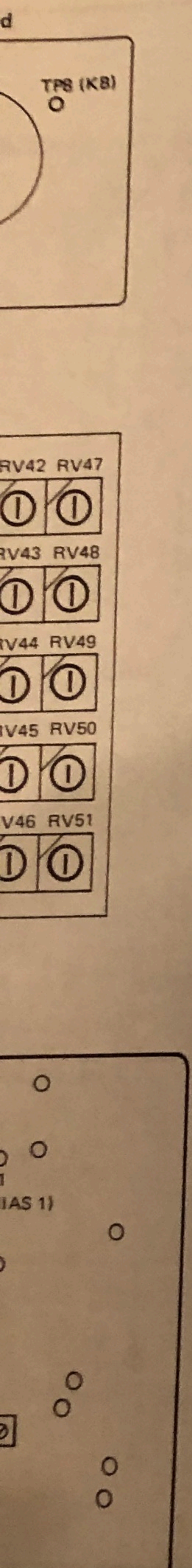


CA board

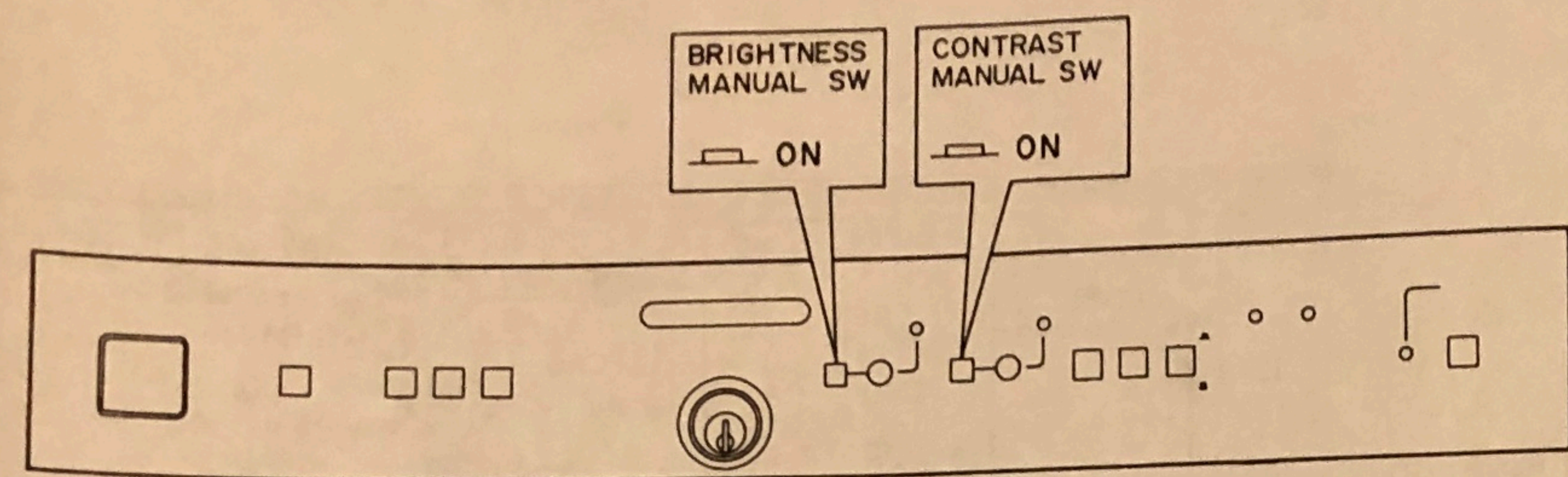


FRONT PANEL

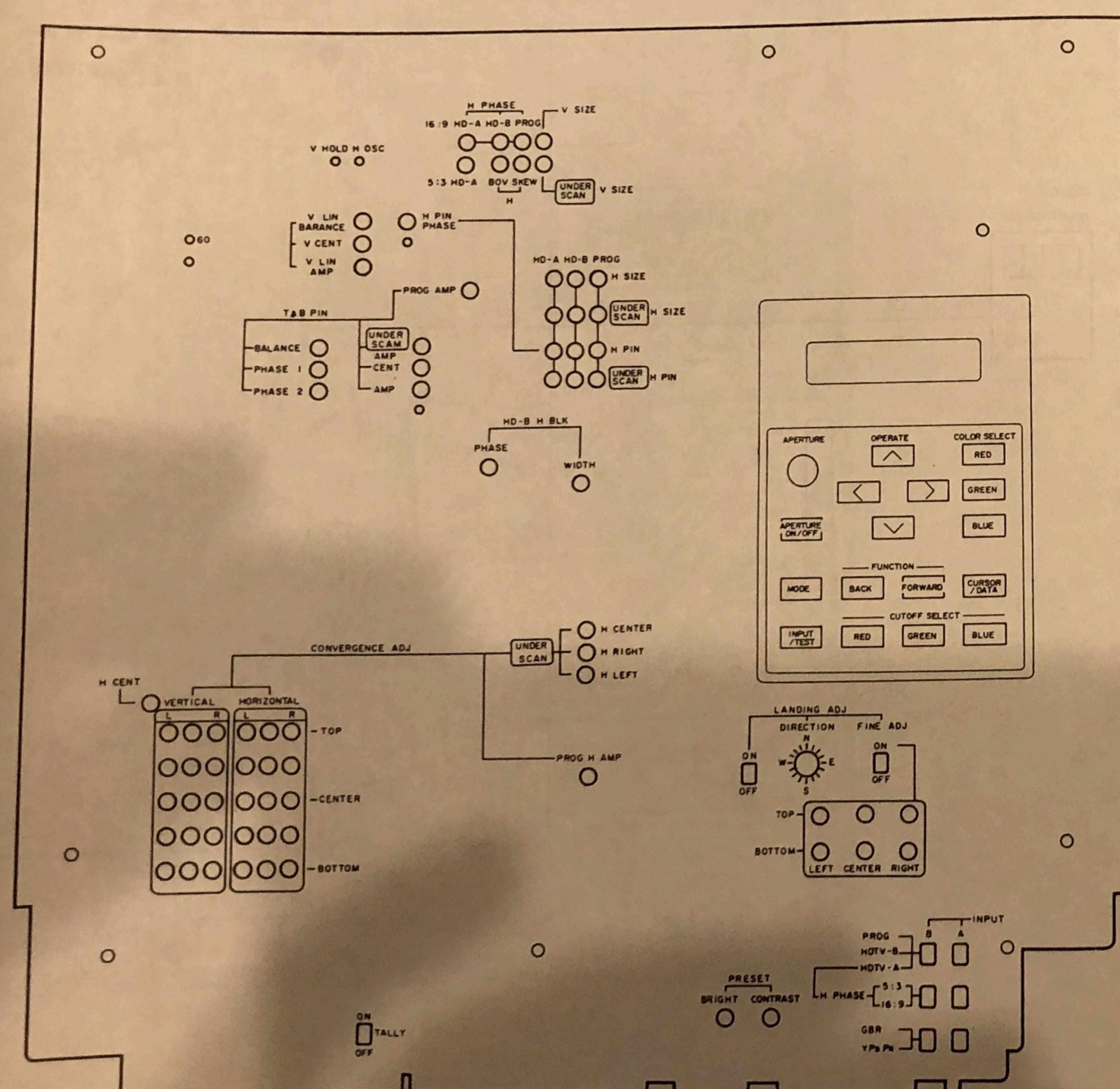




FRONT PANEL



SUB CONTROL PANEL



4-6. SAFETY RELATED ADJUSTMENT

HIGH VOLTAGE ADJUSTMENT

High voltage adjustment is necessary when the components shown below are replaced. Use a high voltage meter for the adjustment.

High voltage blocks, D40, R114, R115, R116, R184 and RV2

1. Receive the white signal and make VR into PRESET mode.
2. Connect a high voltage meter to the anode cap.
3. **Adjust RV2 (VRV) to HV=30 ±0.2 kV**
4. Switch the signal between white and black and be sure the high voltage deviation is less than 0.05kV.

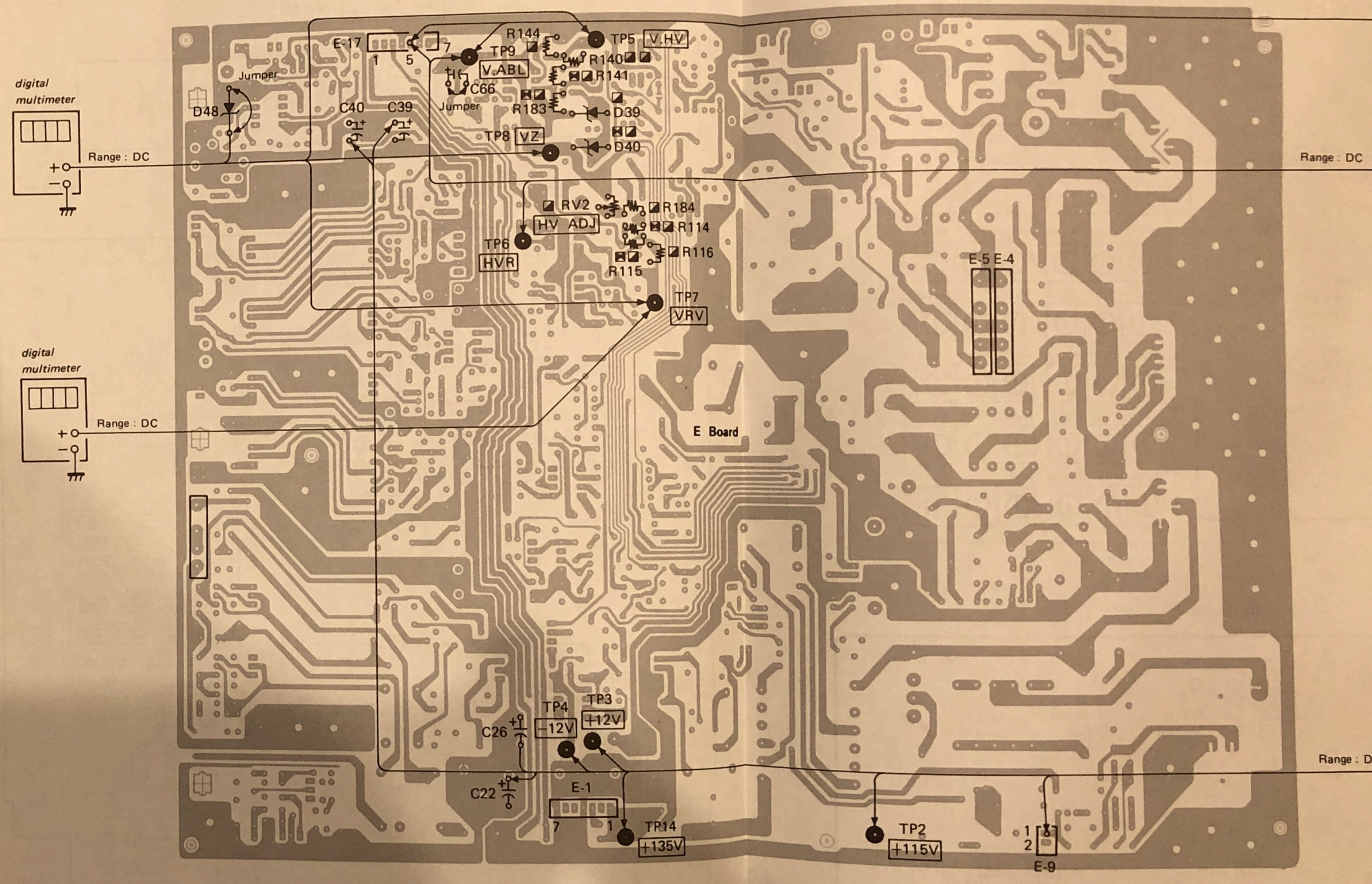
Note: If a high voltage meter is not available, adjust the TP7 (VRV) voltage to 8.40 ±0.05VDC with RV2. Switch the signal alternately and be sure there is no deviation in screen size.

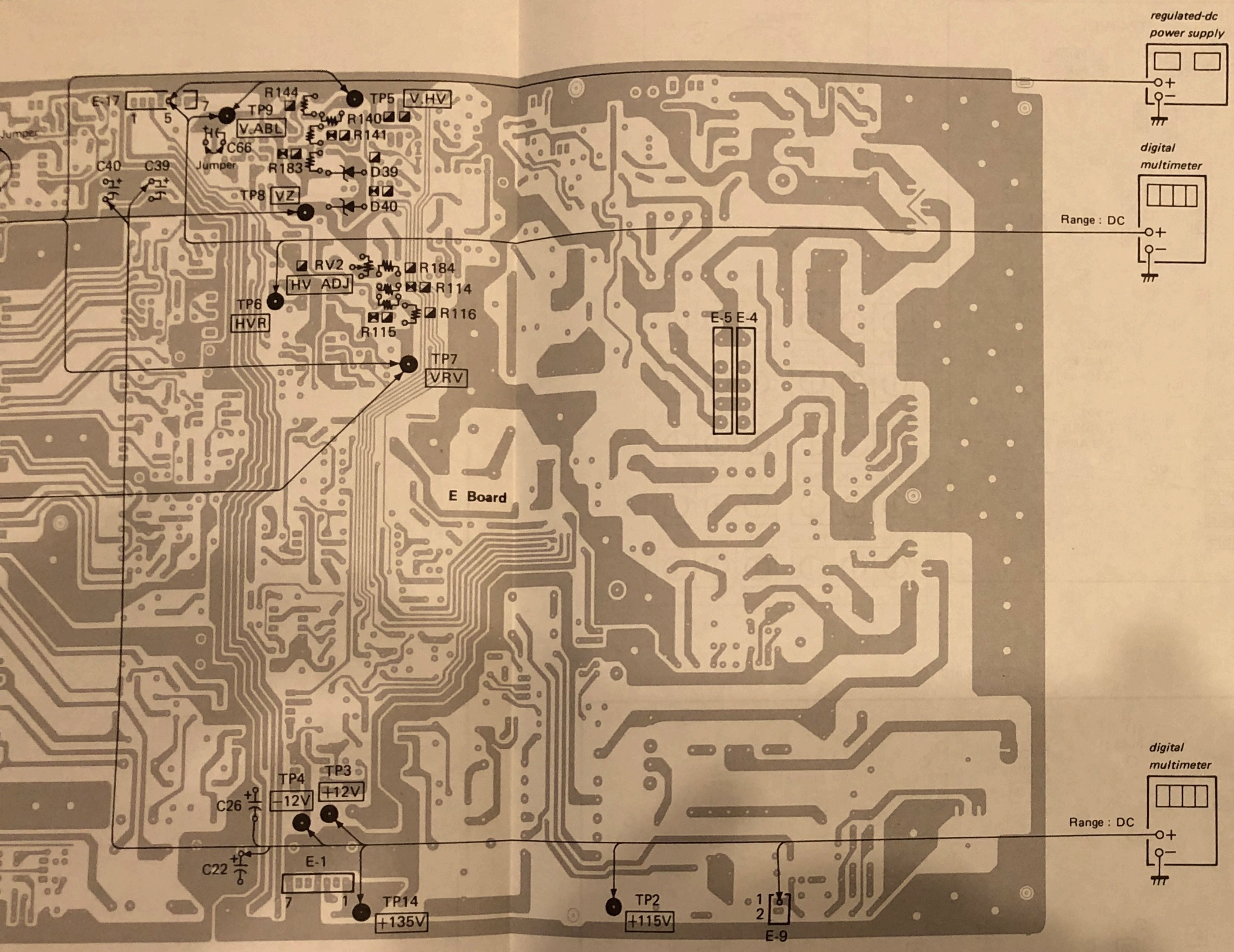
CONFIRMATION OF HIGH VOLTAGE CIRCUIT COMPONENT REPLACEMENT

The specified condition must be satisfied when the following components are replaced:

E board

Part	Description	Condition
D40	μPC574J.HZT33-02	TP8: Within 32.2±1.3VDC
R184	22k±1%	TP7: Adjustable to 8.40 $^{+0.15}_{-0.20}$ VDC
R114	Adjustment resistor	Must be less than 8.70 VDC at RV2 max.
R115	Adjustment resistor	
R116	10k±1%	
RV2	2k±10% Metal grace VR	
R183	Adjustment resistor	TP5: Within 8.90 $^{+0.05}_{-0.10}$ VDC
R140	Adjustment resistor	
R141	Adjustment resistor	
R144	10k±1%	
D39	μPC574J.HZT33-02	
D48	RD6.2EN★	D48 cathode voltage: Within 6.0±0.50VDC
Power supply (TK18)		TP2: Within 115±1VDC
HV block, K board, E board		1. Operation confirmation of the high voltage regulator
D45, R145, 146, E board IC5, R142, 143 D44, R139, D54		2. Confirmation of the HV protector
IC6, E board		3. Confirmation of the Ik protector II
D43, IC5, R137, E board		4. Confirmation of the Ik protector I





CONFIRMATION OF HIGH VOLTAGE PROTECTION CIRCUIT

1. **Operation Confirmation of High Voltage Regulator**
   - HV must be 30 ±0.2 kV.
     (Further, switch the signal from white to black.)
   - The TP6 (HVR) voltage must be 8.40 $^{+0.09}_{-0.40}$ VDC
2. **Confirmation of High Voltage Hold-down Circuit**
   - The voltage of pin ⑤ of the connector E-17 must be 8.40 $^{+0.09}_{-0.40}$ VDC.
   - The raster should not be erased when 8.6 to 8.7 VDC is applied to pin ⑤ of the connector E-17 from the external DC power supply. The hold-down circuit should be active erasing the raster when 9.0 to 9.1 VDC is applied.
3. **Confirmation of Ik Protector Circuit I**
   - When between A and K of D48 is short-circuit and 7.9 to 8.0V is applied from the external DC power supply to TP-9 (ABL), the protector circuit operates and the raster disappears.
4. **Confirmation of Ik Protector Circuit II**
   - When between pin ③ of IC5 and TP-8 is short-circuit and 4.9 to 5.0V is applied from the external DC power supply to TP-9, the protector circuit operates and the raster disappears.
5. **Confirmation ot H STOP**
   1) Disconnect either connector E-4 or E-5 and turn on the power supply.
   2) Be sure that the high voltage protector operates and the raster does not appear.
6. **Confirmation of V STOP**
   1) Remove connector E-14 and set the power supply ON.
   2) Be sure that the high voltage protector operates and the raster disappears.

VOLTAGES OF RESPECTIVE SECTIONS ON E BOARD

The voltages of the respective sections must be as follows (in the white signal preset condition):

1. Pin ① of the connector E-1 (TP14 135V): 135±1VDC
2. Pin ② of the connector E-1 (TP2 115V): 115±1VDC
3. Pin ⑤ of the connector E-1 (TP3 12V): 12±0.6VDC
4. Pin ⑥ of the connector E-1 (TP4 −12V): −12±0.6VDC
5. C22 ⊕ pole: 21±1VDC
6. C26 ⊖ pole: −21±1VDC
7. C39 ⊕ pole: 33±1.5VDC
8. C40 ⊖ pole: −33±1.5VDC
9. Pin ① of the connector E-9: −131±9VDC

4-7. CIRCUIT ADJUSTMENT

CONNECTION METHOD DURING BOARD ADJUSTMENT AND SETTING OF SW

Unless otherwise specified in the following pages, the connection method and switch setting of SW must be made as follows: When only HDTV A is used, it is unnecessary to make adjustments needed for HDTV B or PR.

SETTING POSITIONS OF SWITCHES AND CONTROL KNOBS

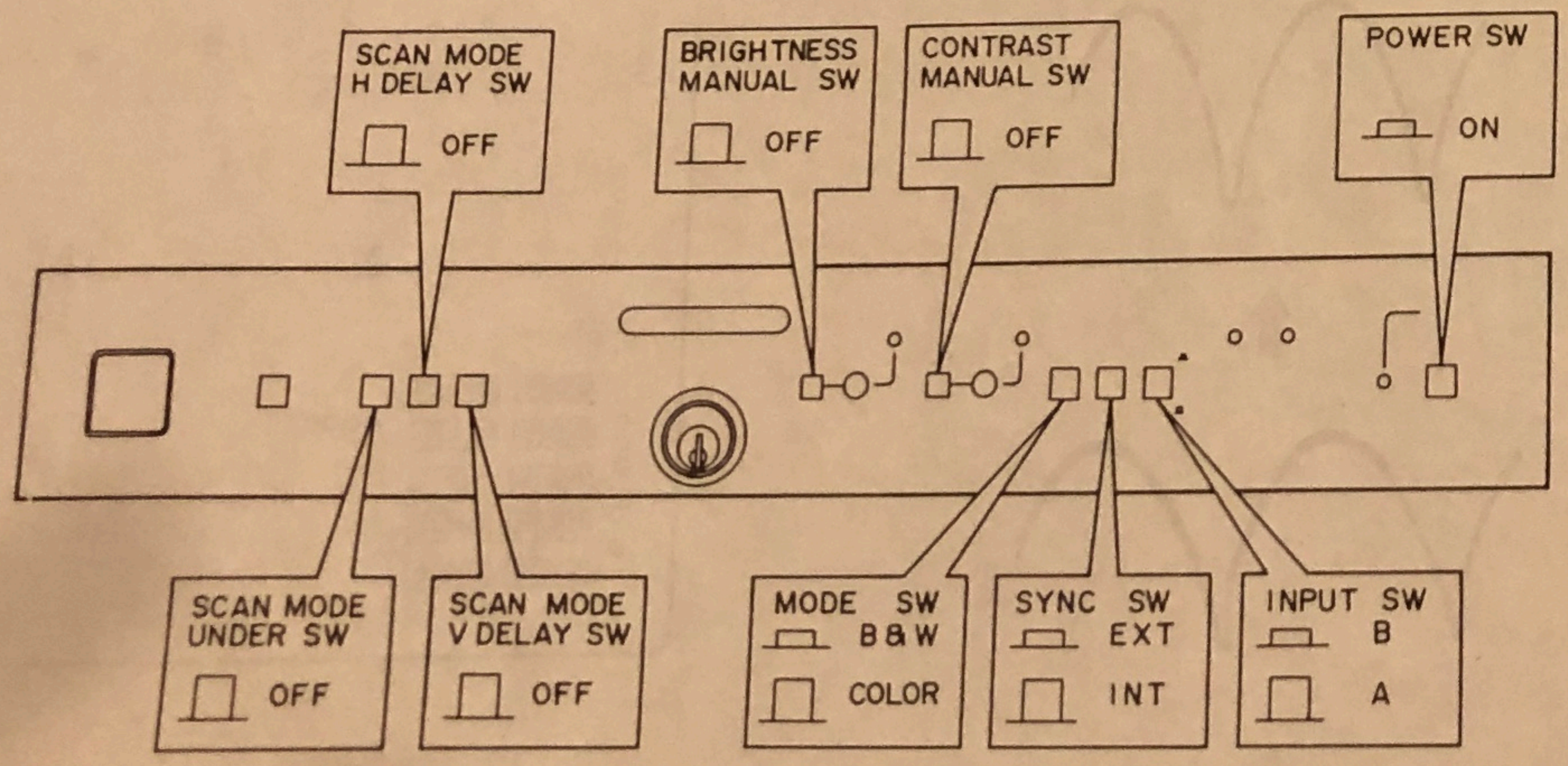
FRONT PANEL

No.	Switch	Setting	Board
1.	INPUT switch	A (⊓)	JA board
2.	SYNC switch	INT (⊓)	JA board
3.	MODE switch	COLOR (⊓)	JA board
4.	CONTRAST MANUAL switch	PRESET (⊓)	JA board
5.	BRIGHTNESS MANUAL switch	PRESET (⊓)	JA board
6.	SCAN MODE V DELAY switch	OFF (⊓)	JB board
7.	SCAN MODE H DELAY switch	OFF (⊓)	JB board
8.	SCAN MODE UNDER switch	OFF (⊓)	JB board

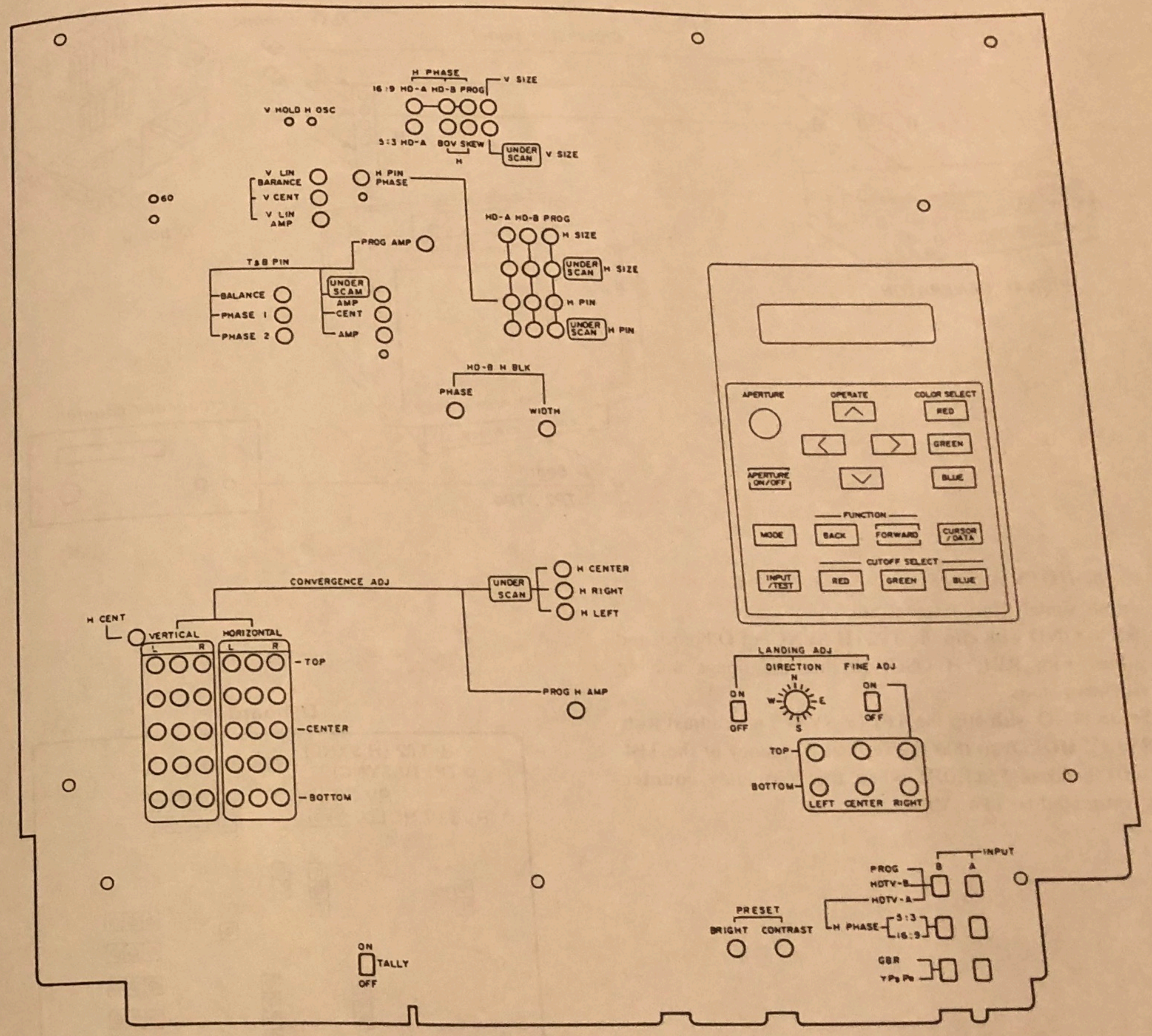
SUB CONTROL PANEL

No.	Switch	Setting	Board
9.	Control unit With the internal signal (at the power on time): TEST MODE	Initial condition	N board
10.	LANDING ADJ ON/OFF switch (SW2)	ON	W board
11.	LANDING ADJ DIRECTION switch (SW1)	Match to monitor setting direction.	W board
12.	LANDING FINE ADJ ON/OFF switch (SW3)	OFF	W board
13.	INPUT A MODE SELECT switch (SW102)	GBR	JA board
14.	INPUT B MODE SELECT switch (SW101)	GBR	JA board
15.	INPUT A H PHASE SELECT switch (SW109)	16:9	JA board
16.	INPUT B H PHASE SELECT switch (SW108)	16:9	JA board
17.	INPUT A SYSTEM SELECT switch (SW113)	HDTV A	JA board
18.	INPUT B SYSTEM SELECT switch (SW110)	HDTV A	JA board
19.	TALLY switch (SW5)	OFF	JB board

FRONT PANEL

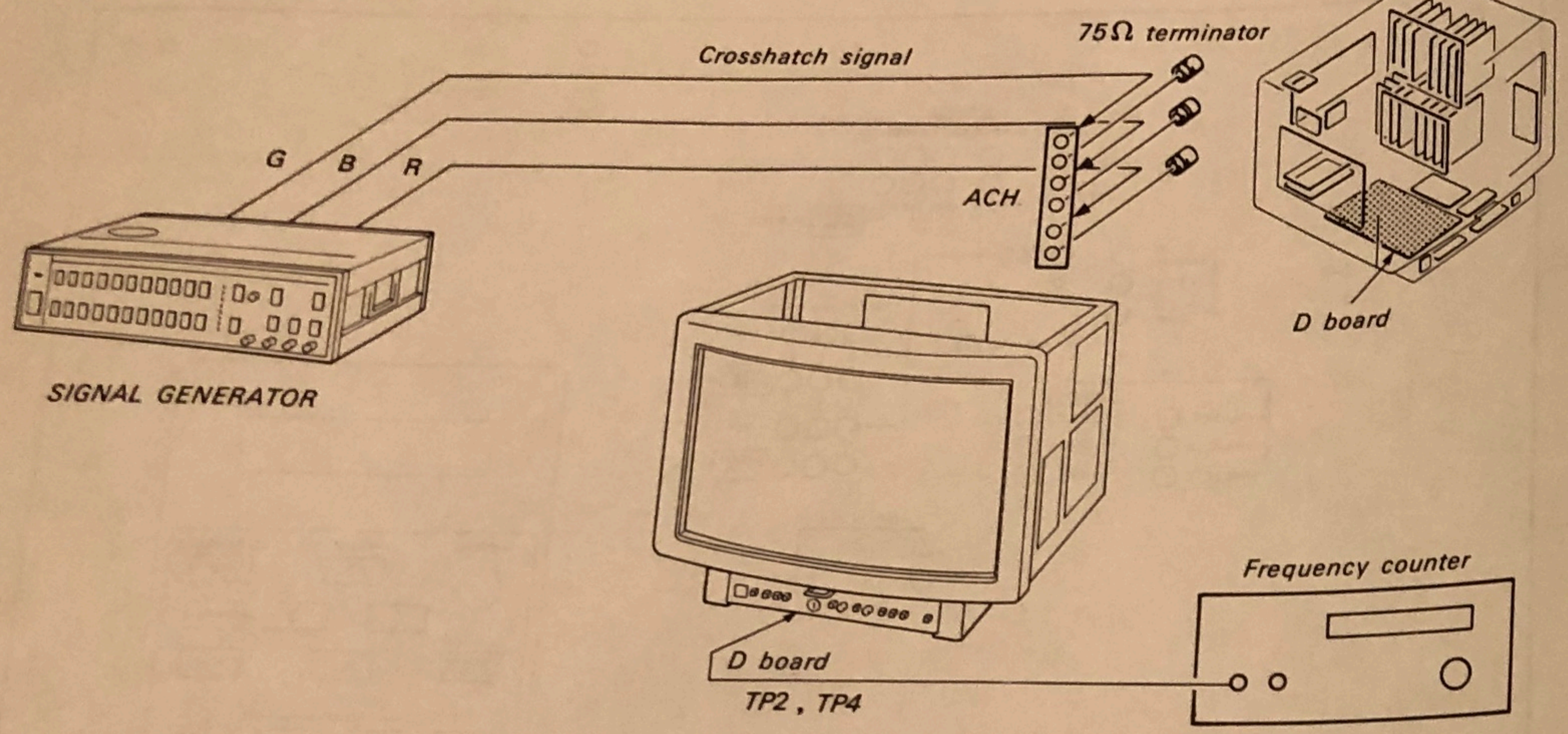


SUB CONTROL PANEL



1. D AND DA, DB, E, R, W BOARDS ADJUSTMENT

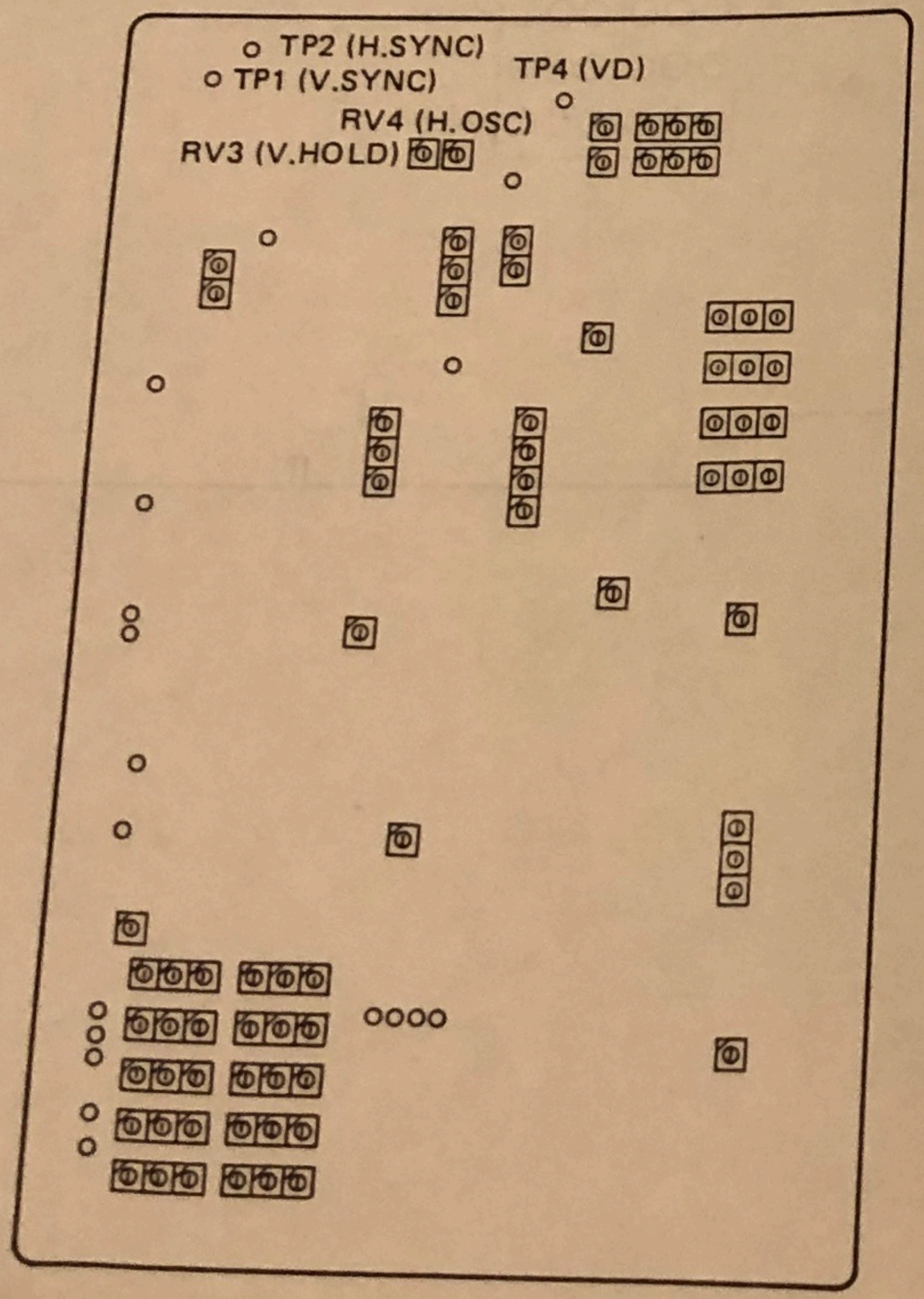
D BOARD fo ADJUSTMENT



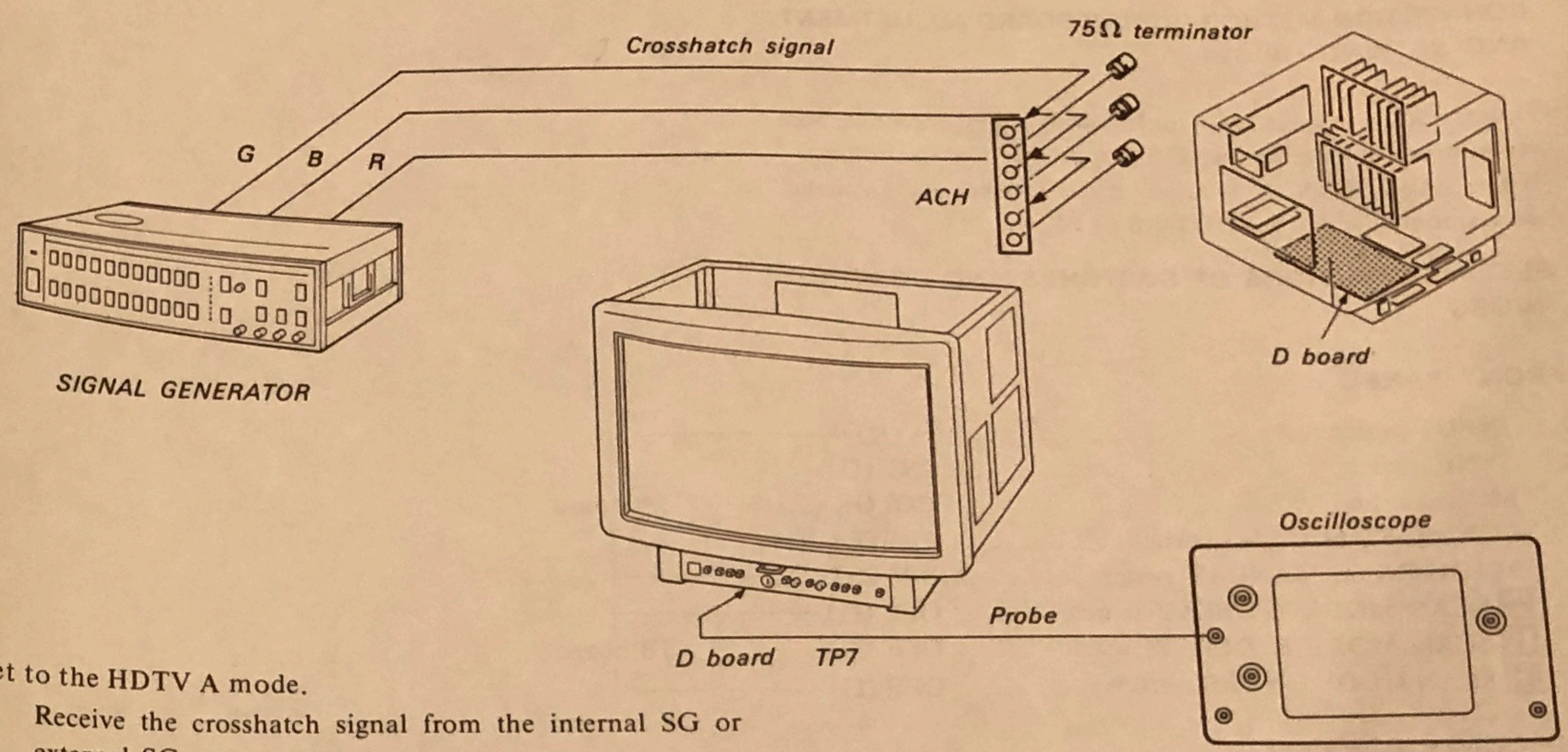
Set to the HDTV A mode.

1. Input signal from external SG.
2. Set to GND with clip the TP2 (H SYNC) of D board, and adjust with RV4 (H OSC) so that the image moving sideways stops.
3. Set to GND with clip the TP1 (V SYNC) and adjust with RV3 (V HOLD) so that the vertical frequency of the TP4 (VD) becomes 55±1.0Hz when the frequency counter is connected to TP4 (VD).

D board



D BOARD V LAMP ADJUSTMENT

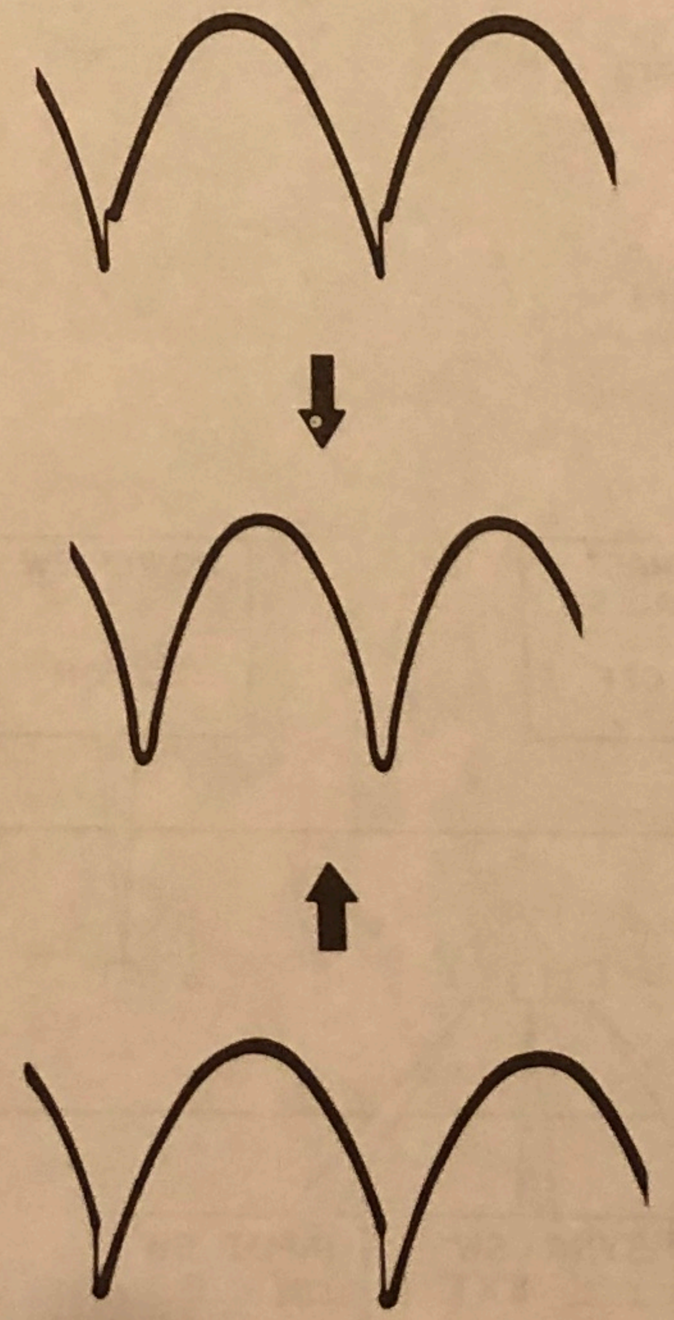


Set to the HDTV A mode.

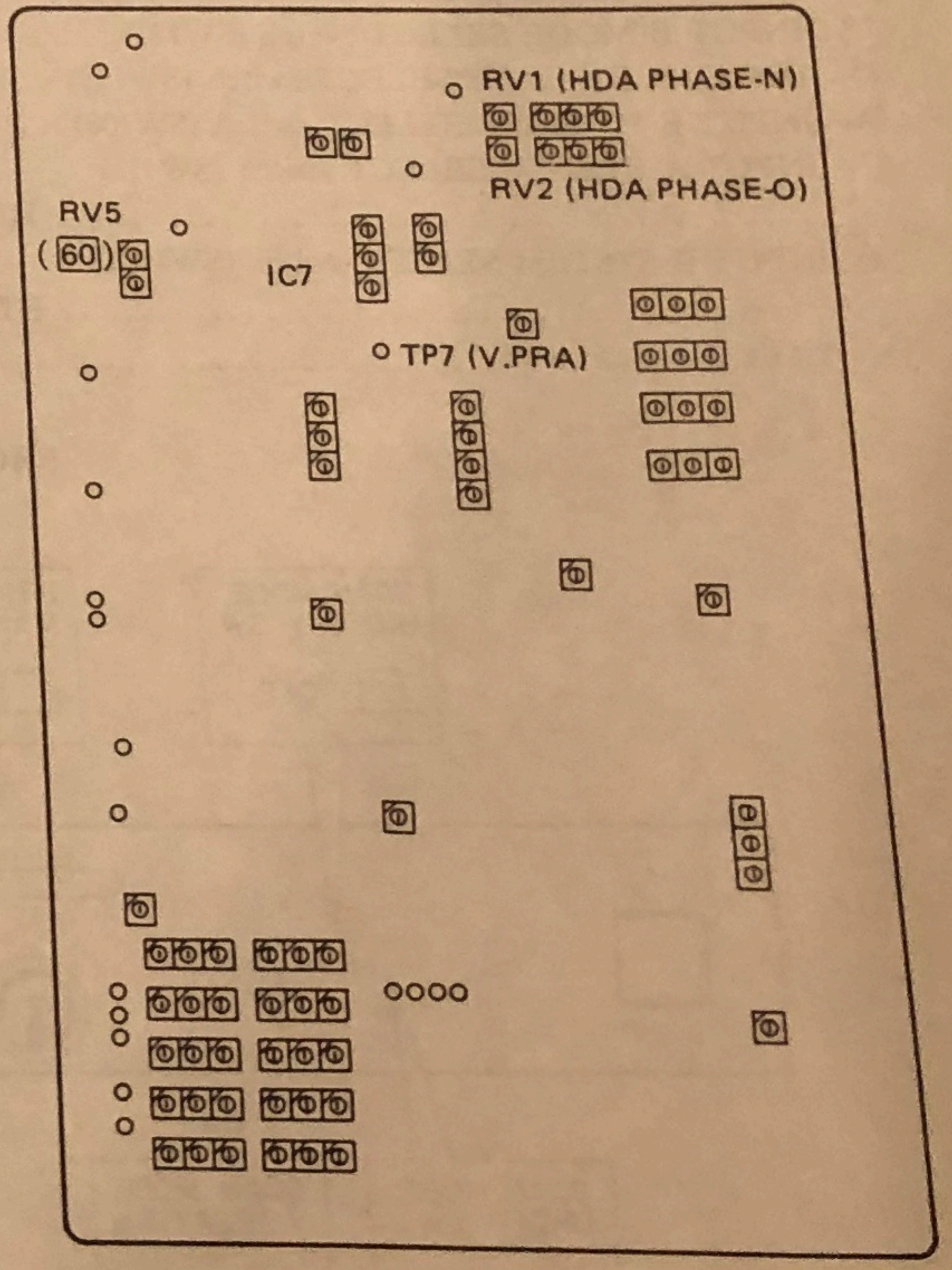
1. Receive the crosshatch signal from the internal SG or external SG.

Note: The picture phase may be different from the internal SG and the receiver image. This phase difference can be matched with HDA H PHASE 16:9 (RV1) or HDA H PHASE 5:3 (setting is by SW on JA board) (RV2) on the subcontrol panel D board.

2. Connect the probe to pin ⑦ (TP7) V.PRA of IC7 of D board, and adjust the VR of [60] (RV5) to display the waveform as shown below.



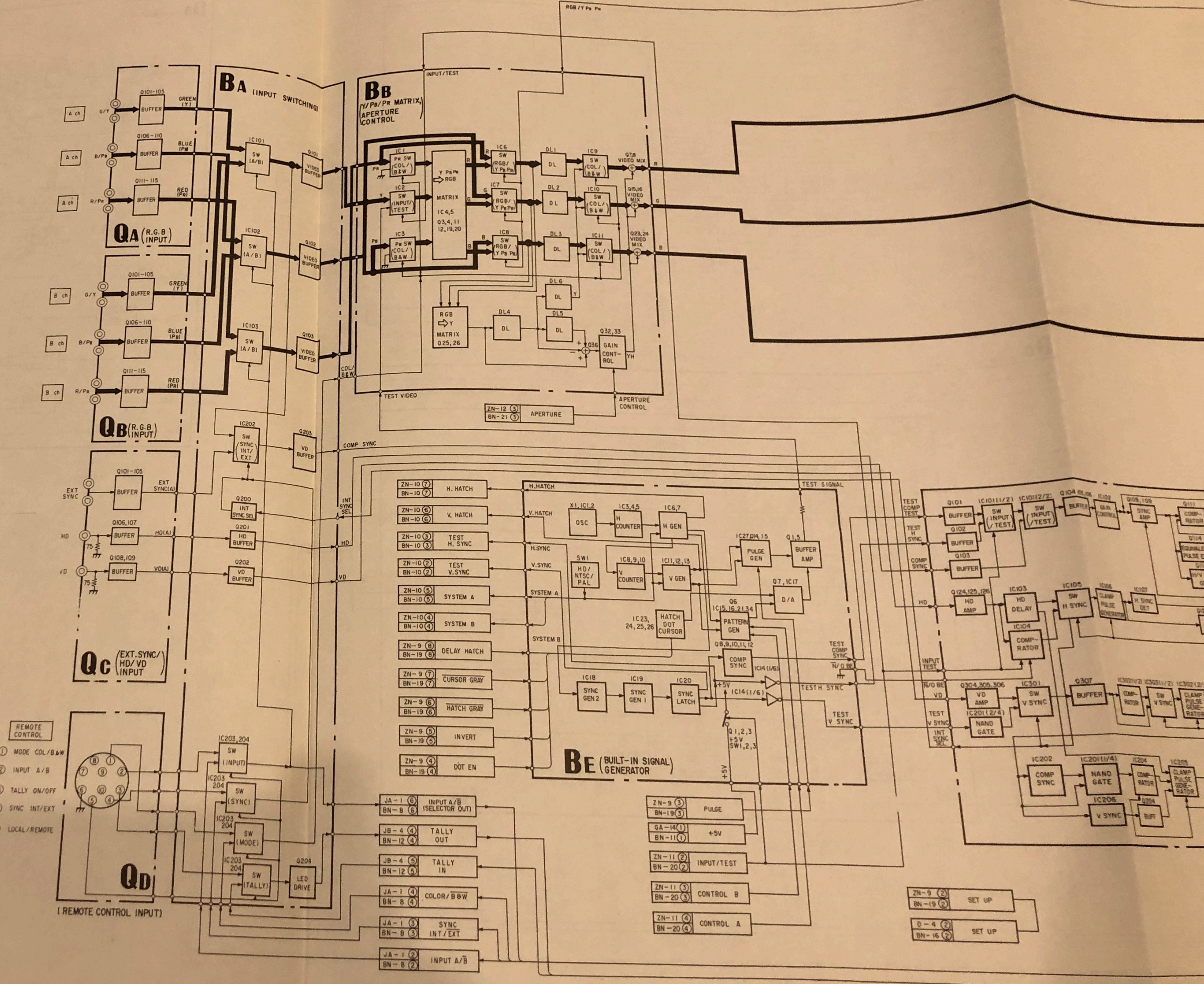
D board


BLOCK DIAGRAMS

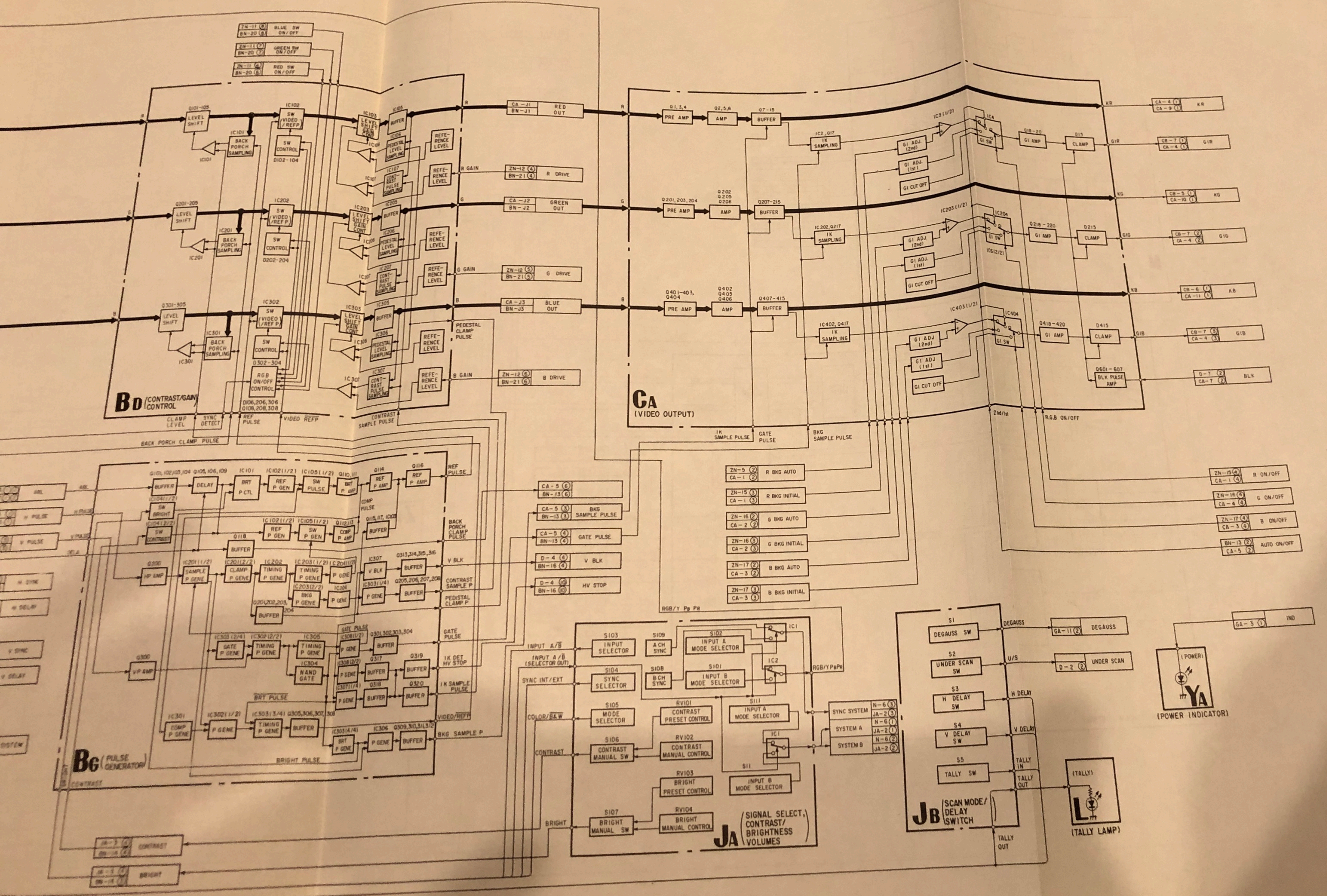
SECTION 5
DIAGRAMS

5-1. BLOCK DIAGRAM
SIGNAL PROCESSING BLOCK DIAGRAM

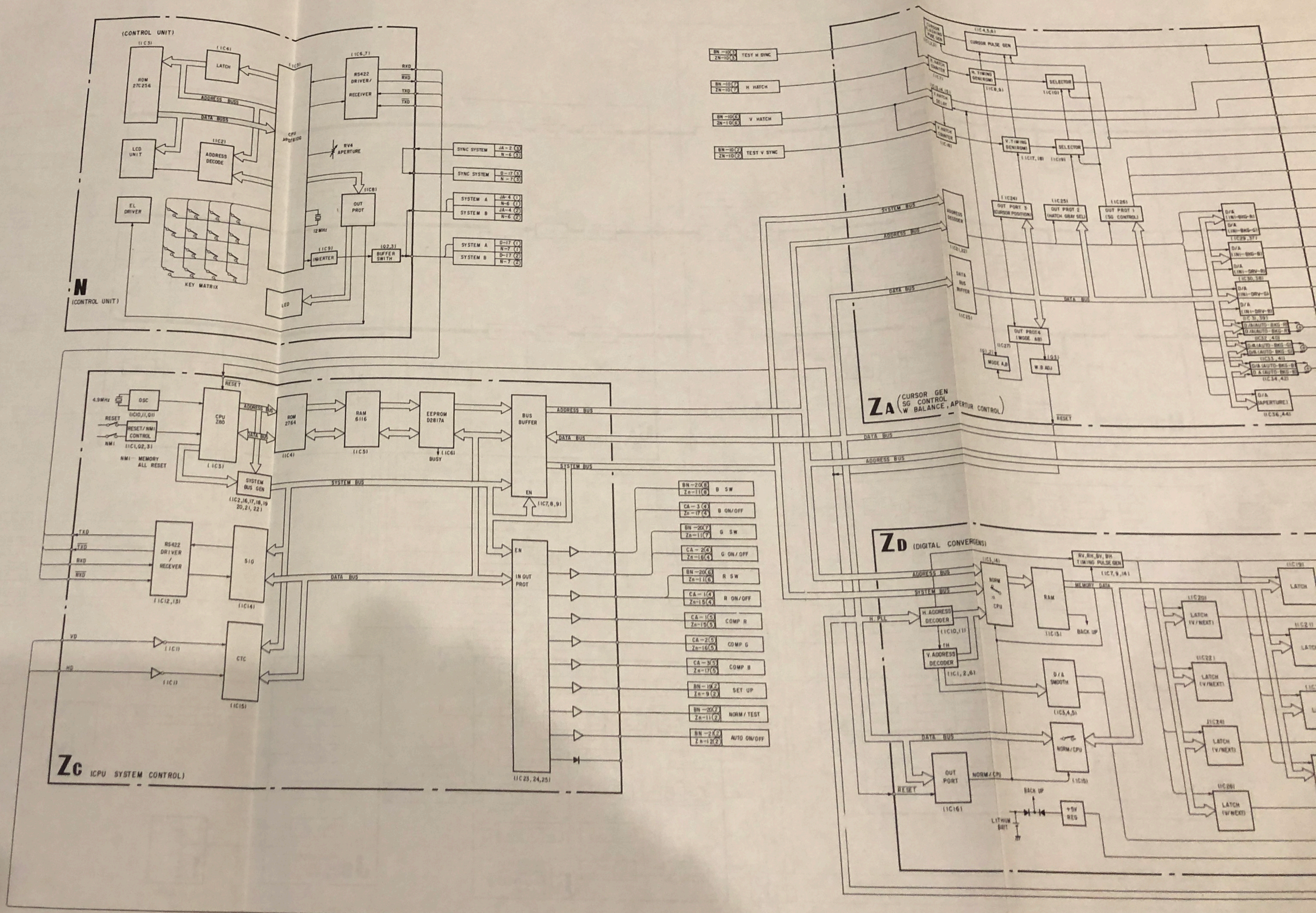


BD (CONTRAST/GAIN CONTROL)
CA (VIDEO OUTPUT)
BE (BUILT-IN SIGNAL GENERATOR)
BF (SYNC PROCESSOR)
BG (PULSE GENERATOR)
JA (SIGNAL SELECT, CONTRAST/BRIGHTNESS VOLUMES)

BLOCK DIAGRAMS
BLOCK DIAGRAMS



CONTROL PROCESSING BLOCK DIAGRAM




ZA (CURSOR GEN, SG CONTROL, W BALANCE APERTUR CONTROL)
ZD (DIGITAL CONVERGENS)
DC (DIGITAL GAIN CONTROL)
ADDRESS BUS
DATA BUS
SYSTEM BUS
CURSOR PULSE GEN
SELECTOR
ADDRESS DECODER
DATA BUS BUFFER
BUS BUFFER
RAM
LATCH
DUAL D/A
FINE H
FINE V
AUX
RESET
BACK UP
+5V REG
+12V

BLOCK DIAGRAMS

